

# The Analog Devices AD6636 Digital Downconverter as a Candidate LWA Receiver Component

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November 9, 2006

## Introduction

The Analog Devices AD6636 is a wideband digital downconverter (DDC) integrated circuit (IC). A DDC accepts digitized data, tunes within the digital passband (shifting the desired frequency to zero Hz), filters to a desired bandwidth, and reduces to sample rate to a value commensurate with the new bandwidth. The AD6636 is of interest because it is available at a cost (currently, \$29.33 in quantities of 1000) that is significantly less than the cost to implement equivalent functionality in FPGAs, and is likely to dramatically reduce associated engineering effort as well.

## Overview of the AD6636

An overview of the part (including a useful block diagram and link to the datasheet) is available at <http://www.analog.com/en/prod/0%2C2877%2CAD6636%2C00.html>. We summarize some relevant features here. The device has four input ports that can accept input data at rates up to 150 MSPS each. Although this is somewhat less than the nominal rate of 256 MSPS described in the LWA Strawman Design (LWA Memo 35), two input ports can be combined with two internal channels processing in tandem, resulting in a configuration in which the part is able to accept two inputs each up 300 MSPS simultaneously. Alternatively, a simple low cost FPGA preprocessor can be used to reduce the sample rate before input to the AD6636. Both methods are discussed later in this memo.

The AD6636 is made up of the following signal processing stages:

- Frequency Translation,
- a 5<sup>th</sup> order CIC filter,
- two cascaded fixed-coefficient FIR and half-band filters,
- three cascaded programmable coefficient sum-of-products FIR filters,
- an Interpolating Half-Band Filter, and
- an Automatic Gain Control block.

Frequency translation is performed using a 32-bit complex NCO which can achieve greater than 110 dB SFDR, and may be bypassed so that baseband inputs can be provided directly from the ADC.

The CIC filter has a programmable decimation rate that can vary from 1 to 32 (only integer values are allowed). The CIC filter is used to lower the sampling rate while providing antialiasing rejection. Following the CIC filter are four additional filters in two stages: FIR1, HB1, FIR2, and HB2. The FIR filters are non-decimating, however, the Half-Band (HB) filters are set to decimate by 2. The second filtering stage can be operated in conjunction with the first stage or bypassed to reduce power consumption.

The programmable filtering is divided into three stages: a Mono-rate RAM Coefficient Filter (MRCF) that consists of a nondecimating FIR filter, two Decimating RAM Coefficient Filters (DRCF) that have programmable decimation rates from 1 to 16 (integer values only are allowed) and may be used

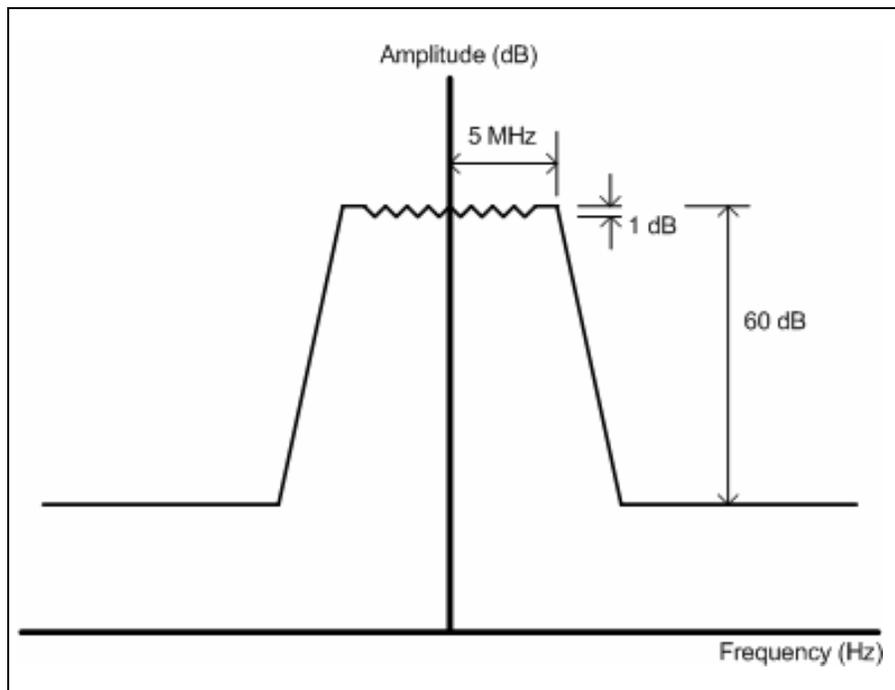
individually or in tandem, followed by the Channel RAM Coefficient Filter which also has a programmable decimation rate from 1 to 16.

Finally, the last filter in the DDC stage is an Interpolate-by-2 half-band filter which up-samples the output of the CRCF. An Output Data Routing Block is used to combine (interleave) samples from more than one channel when using two channels in tandem to achieve a 300 MSPS input, and to distribute samples to an output port. The maximum output sample rate is 34 MSPS.

The AD6636 comes with the filter design software package *SoftCell* that provides a simple means to evaluate a series of filter designs for the part. *SoftCell* also outputs filter parameters in a file that can be loaded onto an evaluation board.

### **LWA Digital Filter Requirements**

We now consider how the AD6636 might be used for the LWA. In this example, we imagine that the LWA ADC samples at 256 MSPS, and we require 10 MHz bandwidth, 60 dB out-of-band suppression, and passband ripple less than 1 dB peak-to-peak. A diagram of these requirements is shown below in Figure 1.



**Figure 1: Filter Requirement for the LWA Digital Receiver.**

Recall that we can achieve this in two ways: (1) operating the AD6636 in interleaved mode using two channels or (2) by using an  $F_s/4$  downconversion processor preceding the DDC. Implementations for both of these techniques will be discussed below.

### **AD6636 in Interleaved Mode**

When operating in Interleaved Mode, the AD6636 must be preceded by a demultiplexer that will split incoming samples into even and odd sample streams. Some ADCs provide this function internally. The two data streams will be input to two ports (either Ports A & B or Ports C & D), and two internal

channels will process samples in tandem. The Output Data Routing Block will perform a complex addition of the even and odd sample channels to create a single signal, which is output as if it had been processed normally as a single channel.

To design the internal filters, first the input sampling frequency is set to a value of 128 MHz, corresponding to the input sample rate for each of the DDC channels. In general, the best filter responses are obtained when the filter stopband is roughly 1/4 to 1/3 of the output sampling rate. Additionally, the filter design software tends to produce more reasonable results when the output sampling rate is a “nice” number (e.g., 12.8 MHz or 16 MHz rather than 14.22222 MHz or 18.285714 MHz). In this example, the overall decimation rate is set to a value of 8, yielding an output sampling rate of 16 MHz per channel (32 MHz when interleaved). The PLL Adjusted Clock (which is the internal DDC clock that is used to process filter data) is set to a value of 192 MHz. Setting the internal PLL clock operate faster than the incoming sample rate means that a larger number of filter taps can be processed by the DDC, and hence, a narrower transition region or greater stopband rejection can be achieved.

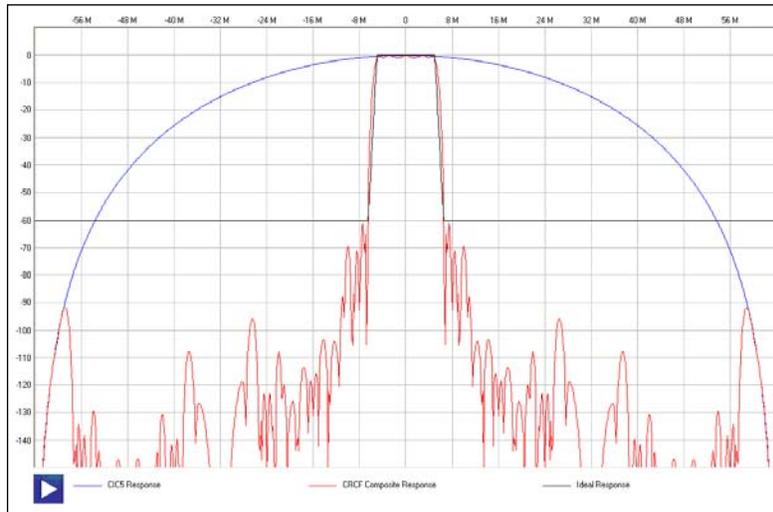
The transition region of the filter is set to Equal Ripple, as the Root Raised Cosine mode generally results in filters that have relatively large sidelobes. The passband frequency is set to 5 MHz (this is the lowpass bandwidth), and the Ripple is set to 0.5 dB. The stopband is set to 6.5 MHz and a rejection of -60 dB. Narrower transition regions are possible, but at the expense of increased sidelobe levels in the filter. The CRCF, DRCF, and both FIR filters are all enabled.

The filter design software produces a number of possible outputs, but the option that produces the best response is:

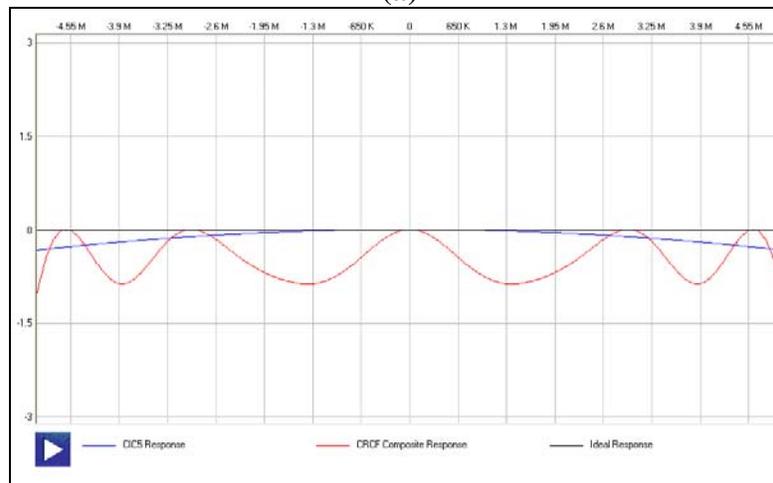
$$CRCF = 1, DRCF = 1, HB2 = 2, HB1 = 2, \text{ and } CIC5 = 2$$

These numbers represent the decimation rates for the various filters. The combination above yields a decimation rate of 1 for the CRCF filter, a decimation rate of 1 for the DRCF filter, a decimation rate of 2 for both Half-Band filters, and a decimation rate of 2 for the 5<sup>th</sup> order CIC Filter. Setting the CRCF Taps and DRCF Taps to 12 each yields the filter response shown below in Figure 2.

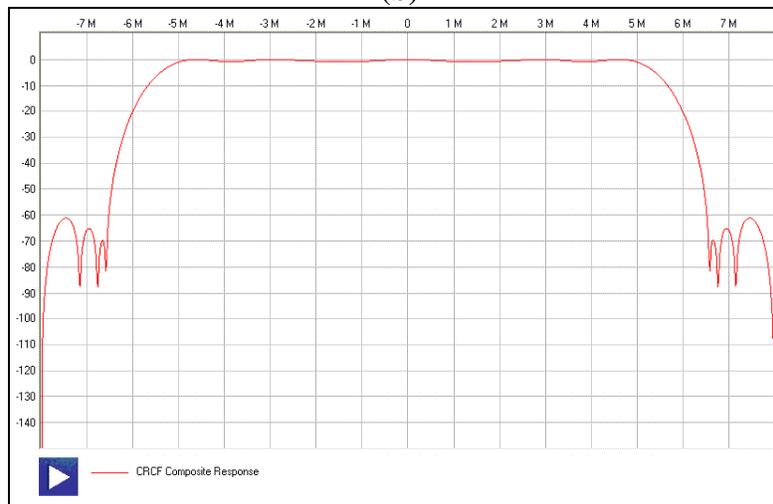
Note that all filter parameters (ripple, bandwidth, narrowness of the transition region, and sidelobe level) can be traded off against each other, so this example represents only one potential configuration of the DDC part.



(a)



(b)



(c)

**Figure 2: Example design for the AD6636 in Interleaved Mode. (a) Overall frequency response of the filter, (b) Passband ripple response of the filter, and (c) Close-up view of the passband.**

## AD6636 in $F_S/4$ Mode

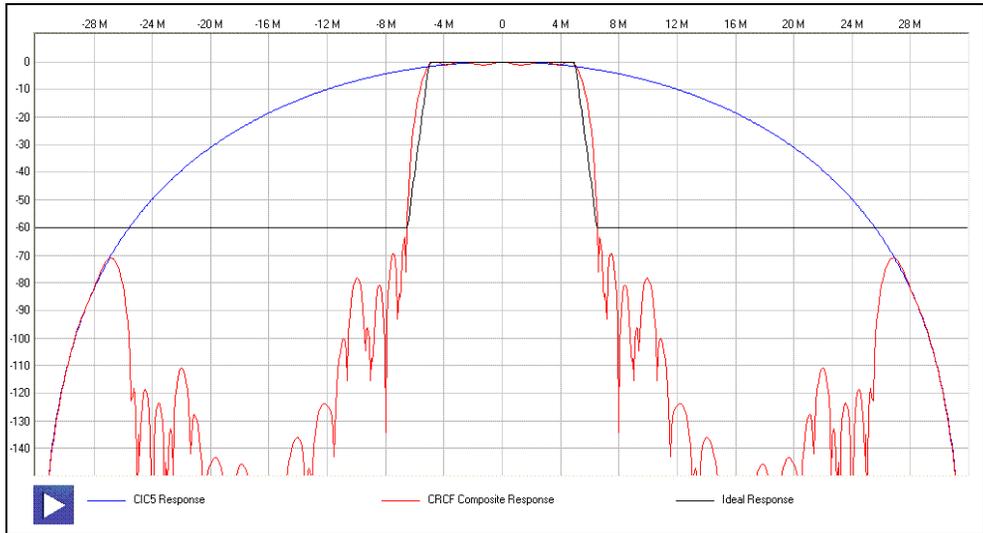
An alternative to interleaving ADC samples prior to the DDC is to perform  $F_S/4$  downconversion to obtain a complex baseband signal that can be decimated to a lower rate.  $F_S/4$  downconversion requires no multipliers – exploiting the fact that a spectral shift equal to  $1/4$  the sample rate is equivalent to multiplication by  $+1, +j, -1, -j, +1, \dots$  – and subsequent filtering is necessary only if required to satisfy the Nyquist criterion after decimation. Thus,  $F_S/4$  downconversion can be implemented in a relatively low-cost FPGA. If we assume reasonably tight analog filtering to form a 20-80 MHz passband, then  $F_S/4$  downconversion after sampling at 256 MSPS will result in 64 MHz being shifted to zero Hz, and the band edges will be at -44 MHz and +14 MHz. Thus, the sample rate could be reduced from 256 MSPS to 128 MSPS with no further filtering. The two resulting data streams (i.e., I and Q) will be input to two ports (either Ports A & B or Ports C & D) on the DDC part, and the DDC will be configured to internally combine the inputs into complex samples prior to processing.

To design the internal filters, first the input sampling frequency is set to a value of 128 MHz. As before, the best filter responses are obtained when the filter stopband is roughly  $1/4$  to  $1/3$  of the output sampling rate. Thus, the overall decimation rate is set to a value of 4, yielding an output sampling rate of 16 MHz. The PLL Adjusted Clock is set to a value of 192 MHz. The transition region of the filter is set to Equal Ripple, with a passband frequency of 5 MHz, 0.5 dB Ripple, and a stopband at 6.5 MHz with a rejection of -60 dB. The CRCF, DRCF, and both FIR filters are all enabled.

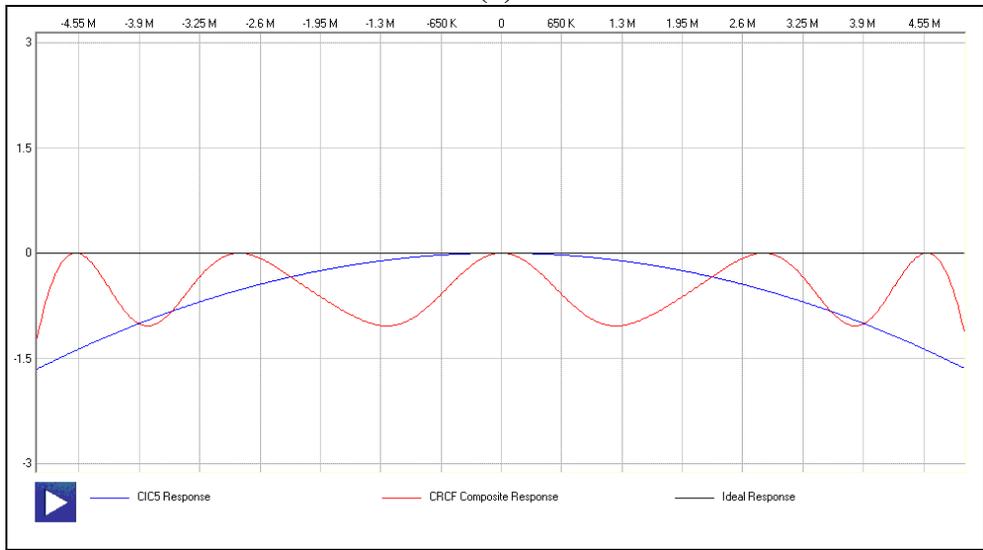
The filter design software produces a number of possible outputs, but the option that produces the best response is:

$$CRCF = 1, DRCF = 1, HB2 = 2, HB1 = 1, \text{ and } CIC5 = 4$$

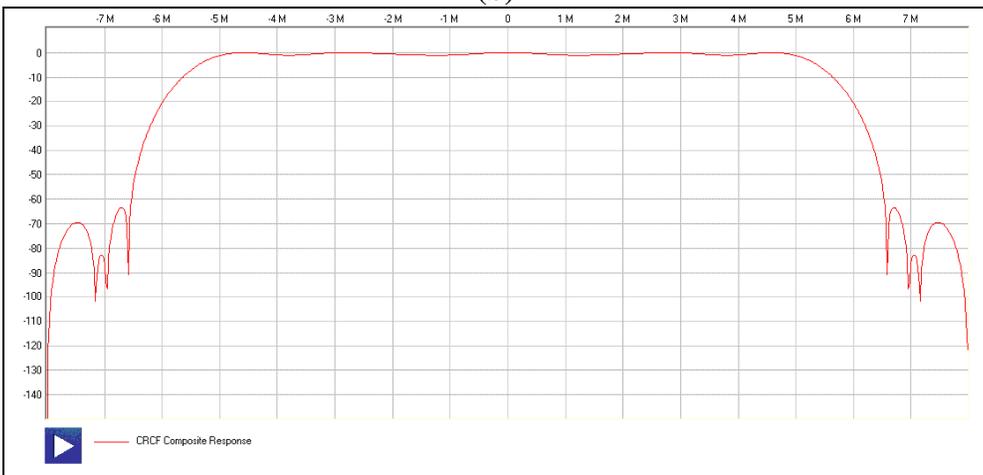
Setting the CRCF Taps and DRCF Taps to 12 each yields the filter response shown below in Figure 3.



(a)



(b)



(c)

**Figure 2: Filter response when operating the AD6636 in  $F_S/4$  Mode. (a) Overall frequency response of the filter, (b) Passband ripple response of the filter, and (c) Close-up view of the Filter Passband.**