Silicon Pixel Capacitance

Grant Gorfine [a] Martin Hoeferkamp [a] Geno Santistevan [a]
Sally Seidel [a,1]

[a] *New Mexico Center for Particle Physics, University of New Mexico, Albuquerque, NM 87131, USA*

Abstract

Capacitance measurements have been made on silicon pixel sensors of types n^+-on-n, p^+-on-n, and n^+-on-p. The arrays test a variety of implant and gap widths, and the n^+ on n devices test several p-stop designs. The measurements examine inter-pixel and backplane contributions and include studies of temperature dependence. Measurements were made before and after irradiation with fluences relevant to LHC experiments and Fermilab Tevatron Run 2.

Key words: Silicon detectors; Capacitance

1 Introduction, Test Structures, and Measurement Procedure

The capacitance is a sensitive parameter in the operation of a silicon tracking detector, as it directly affects the noise and crosstalk. We have measured and simulated the inter-pixel capacitance of a variety of n-on-p, p-on-n, and n-on-n pixel test structures of dimensions comparable to those used in or planned for several collider experiments. The n-on-p and p-on-n test structures each have six 3×9 arrays of pixels. The center pixel in each array is isolated, and the surrounding pixels are connected together. This allows all the surrounding pixels to be biased with a single probe. The pitch is 50 μm $\times$ 536 μm. The p-bulk detectors have a p^+ isolation implant (also know as a p-stop)(1) surrounding the n^+ implants. The widths of the pixel implants (p^+ in the case of n-type bulk and n^+ in the case of p-type bulk) are systematically varied for each array. For the p-type detectors, the p-stop widths and the gaps (unimplanted

[1] Presenter. E-mail: seidel@glueball.phys.unm.edu.

regions) between the n^+ implants and p-stops are also varied in the six arrays. The values of the pixel implant width (denoted as W), the p-stop width (denoted as P), and the gap G between p-stop and n^+ implant are listed in Table 1 for each of the arrays. Also listed is the parameter g, which is the total gap between implants. For the n-type devices, $g = G = 50 - W$, while for the p-type ones, $g = 2G = 50 - W - P$. There is also an unimplanted region 100 μm wide between the edge of the array and the guard ring, which is 30 μm wide. The thickness of the detectors is 300 μm. Five p-on-n and five n-on-p test structures were studied.

Table 1 Dimensions of the p-on-n and n-on-p test structure pixel arrays, in microns.

Array No.	p-on-n			n-on-p			
	p^+ Implant Width ("W")	Gap Width ("G")	Total Gap ("g")	n^+ Implant Width ("W")	p-stop Width ("P")	Gap Width ("G")	Total Gap ("g")
2	38	12	12	38	4	4	8
3	32	18	18	32	6	6	12
4	23	27	27	23	8	8 & 11‡	19
5	20	30	30	20	10	10	20
6	14	36	36	14	12	12	24

‡In p-type Array 4, there was an error in the layout that caused the gap to be 8 μm wide on one long side and 11 μm wide on the other.

The n-on-n test structures, nominally 300 μm thick, contain 11 arrays, each with variations in implant widths and p-stop design. Their pitch is $50\mu\text{m} \times 400\mu\text{m}$. Table 2 summarizes their features. Each array includes 33 pixels in a 3×11 matrix. The center three pixels are isolated while the surrounding ones are all connected together. Three p-stop designs are included in the n-on-n arrays: the "atoll" design, which has a p-stop ring around each pixel; the "common" design, in which a continuous p-stop forms a grid around the pixels; and the "combined" design, which uses both atoll and common p-stops.

Capacitance measurements were made with an HP4284A LCR meter, which supplies a small AC test signal (set to 250 mV RMS) on the HIGH terminal. The amplitude and phase are measured on the LOW terminal. To measure the inter-pixel capacitance between a pixel of interest and all or some of the surrounding pixels, the pixel of interest is connected to the LOW terminal via a low parasitic capacitance probe, and the HIGH terminal is connected to the neighbors of interest. Prior to taking a measurement, an OPEN correction is done on the HP4284A LCR meter to measure all the parasitic capacitances in the setup, including cable and probe contributions,

Table 2 Summary of the dimensions of the n-on-n arrays, in microns. W is the n^+ implant width; A, the metal width; P, the p-stop width; G, the gap between n^+ and p^+ implants; H, the gap between neighboring p^+ implants; and g, the total gap between implants. For devices with common p-stops, $g = 2G = 50 - W - P$; for devices with atoll p-stops, $g = 2G + H = 50 - W - 2P$; for devices with combined p-stops, $g = 2G + 2H = 50 - W - 3P$.

Array No.	p-stop Design	W	A	P	G	H	g
1	Atoll	23	18	5	6	5	17
2	Atoll	23	29	5	6	5	17
3	Atoll	16	12	5	6	12	24
4	Atoll	15	12	5	10	5	25
5	Atoll	19	14	5	8	5	21
6	Combined	13	12	5	6	5	22
7	Common	33	25	5	6	N/A	12
8	Common	28	23	10	6	N/A	12
9	Common	23	18	15	6	N/A	12
10	Common	24	19	10	8	N/A	16
11	Common	20	15	10	10	N/A	20

while the sensor is biased. The measurement is stored and used as the reference point in subsequent measurements.

The statistical error on any particular capacitance measurement reported here is 3 fF, a value taken from the standard deviation of a distribution of identical measurements made on a typical unirradiated test structure at a representative frequency (1 MHz) and voltage (200 V). As a systematic error we take 1 fF, which is a conservative measure of the voltage dependence of the OPEN correction on a typical capacitance measurement. The accuracy of the capacitance measurement, as given by the LCR meter specifications, is 3 fF. We combine these three errors in quadrature to get 5 fF as the total measurement error on unirradiated sensors. The irradiated sensors incur one additional systematic error of average value 6 fF. This is associated with extrapolation of their capacitance to a voltage regime in which it is expected to approximate its asymptote, for sensors whose radiation damage prevented them from being operated at voltages that high.

2 Measurements on p-on-n and n-on-p Devices

Measurements were made on unirradiated and irradiated p-on-n and n-on-p structures at frequencies ranging from 3 kHz to 1 MHz. The 1MHz data are most relevant to planned or likely future readout systems at LHC and Tevatron experiments. Tables 3 and 4 summarize the capacitances in the flat C-V region beyond full depletion. No variation with frequency was seen in capacitance above full depletion for unirradiated sensors.

Table 3 Measured inter-pixel capacitance of unirradiated and irradiated (4.8×10^{13} n_{eq}/cm^2 fluence) p-on-n detectors.

Array No.	p^+ Implant Width (μm)	$C^{unirrad}$ (fF)	C^{irrad} (fF)
2	38	115 ± 5	114 ± 7
3	32	94 ± 5	96 ± 6
4	23	73 ± 5	71 ± 7
5	20	66 ± 5	66 ± 7
6	14	56 ± 5	56 ± 7

Table 4 Measured inter-pixel capacitance of unirradiated and irradiated (4.8×10^{13} n_{eq}/cm^2 fluence) n-on-p detectors.

Array No.	n^+ Implant Width (μm)	$C^{unirrad}$ (fF)	C^{irrad} (fF)
2	38	200 ± 5	218 ± 5
3	32	153 ± 5	159 ± 9
5	20	103 ± 5	116 ± 10
6	14	88 ± 5	100 ± 14

The results are consistent with those reported for a similar measurement(2) of silicon strip sensors; in particular, after irradiation the dependence of the capacitance upon the bias voltage is significantly increased. The capacitance of the irradiated sensors was seen to depend more strongly on the signal frequency than was the case for the unirradiated detectors. This frequency dependence phenomenon has been described elsewhere(3; 4) for backplane capacitance.

We have investigated whether the capacitance varies linearly with the width-to-pitch ratio ($W/\wp$) as has been shown (5) to be the case for silicon strip sensors. We take 50μm to be the relevant pitch in this study, as the capacitance between the short sides of adjacent pixels is only about 10% of the capacitance between the long sides.

Because the pitch is the same in all of the sensors that we studied, we are not able to investigate explicit dependence of capacitance upon pitch but instead test whether the relationship to the width is linear. Figure 1 shows that a linear fit describes the data adequately up to a width of 32μm. This is consistent with the validity region ($W/\wp < 0.6$) given in Reference (5). However, a linear relationship fails to describe the data for larger implant widths in p-type sensors. Figure 1 shows that an improved fit is achieved for the function

$$C_{\text{inter-pixel}} = A + BW/\wp + D/g. \tag{1}$$

Here W, $\wp$, and g are the width, pitch, and total gap between implants, respectively, as listed in Table 1. For the p-on-n and n-on-p test structures, the p-stop width is proportional to the gap width, so g is proportional to $50 - W$; hence it is possible to plot the result as a function of W.

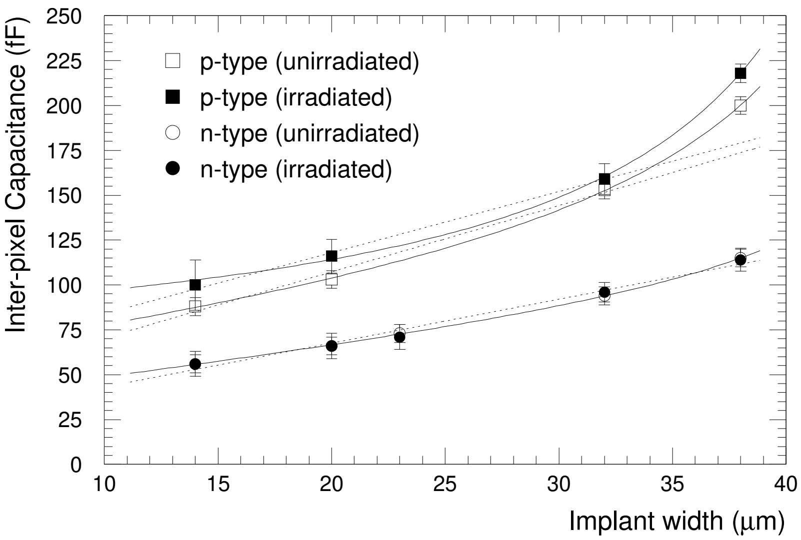

Fig. 1. Inter-pixel capacitance versus width for irradiated (4.8×10^{13} $\mathrm{n_{eq}/cm^2}$ fluence) and unirradiated p-on-n and n-on-p sensors of pitch 50μm. Fits to a straight line and to the function given in Equation (1) are shown.

The setup for the backplane capacitance measurement is similar to that for the inter-pixel measurement in that the LOW terminal is connected to the center pixel. The HIGH terminal, however, is not connected to the surrounding and neighboring pixels but is connected to the backside of the sensor. The results of backplane capacitance measurements made on unirradiated p-on-n and n-on-p pixels are summarized in Tables 5 and 6. The typical pixel designs represented in this study indicate that the total pixel capacitance includes backplane and inter-pixel capacitances in a ratio of about 10–25% for both p-on-n and n-on-p devices.

Table 5 Measured and simulated values of the backplane capacitance of a p-on-n sensor. The total error on each measurement is conservatively estimated at 5fF. The uncertainty on the simulation results is ±20%.

Array No.	Measured C (fF)	Simulated C_{IES2D} (fF)	Simulated C_{IES3D} (fF)
2	15	10.4	13.4
3	15	10.3	13.1
4	11	10.3	12.7
5	15	10.3	12.6
6	13	10.2	12.2

Table 6 Measured values of the backplane capacitance of an n-on-p sensor. The total error on each entry is conservatively estimated at 5fF.

Array Number	Measured C (fF)
2	18
3	16
4	11
6	21

3 Simulations of p-on-n Devices

Electrostatic simulations of the inter-pixel and backplane capacitances of the p-on-n devices were carried out to aid in the interpretation of the capacitance measurements. The two-dimensional electrostatic simulators, HSPICE IES Electro, were used. The results of these studies are shown in Tables 5 and 7. Table 8 shows the predicted contribution of the higher order parallel capacitance terms. The results of the two simulations bracket the measured values for the inter-pixel capacitance. A comparison of the two simulators leads us to assign an uncertainty of ±35% to the simulation result. The calculation was repeated with the three-dimensional electrostatic field simulator IES Coulomb. The three-dimensional model improves on the two-dimensional one by adding contributions to the capacitance associated with coupling to the implant's ends and with diagonal couplings. These contributions were then summed to predict the total inter-pixel capacitance associated with the nearest neighbors. These three-dimensional results are summarized in Tables 5 and 7 and agree with the measurements to an accuracy of better than 30%.

Table 7 Simulated values of inter-pixel capacitance of unirradiated p-on-n detectors.

Array Number	p^+ Implant Width (μm)	Simulated $C^{\rm unirrad}_{\rm HSPICE}$ (fF)	Simulated $C^{\rm unirrad}_{\rm IES2D}$ (fF)	Simulated $C^{\rm unirrad}_{\rm IES3D}$ (fF)
2	38	130	109	124
3	32	115	91	111
4	23	95	78	93
5	20	89	72	87
6	14	75	66	76

Table 8 Higher order contributions to the inter-pixel capacitance of a p-on-n sensor as simulated with the IES Coulomb three-dimensional electrostatic field solver. Cp is the capacitance to the nearest pair of neighbors; Cp2, to the next-to-nearest pair; and Cp3, to the next-to-next-to-nearest pair.

Array Number	p^+ Implant Width ("W") (μm)	Gap Width ("G") (μm)	Cp (fF)	Cp2 (fF)	Cp3 (fF)
2	38	12	46	5.30	3.30
3	32	18	37	5.25	3.25
4	23	27	31	5.20	3.15
5	20	30	28	5.15	3.10
6	14	36	25	5.00	3.05

4 Measurements of the n-on-n Devices

The n-on-n test structures were fabricated by two manufacturers, CiS and Seiko. Where necessary, we have identified the devices by their vendor. Capacitance measurements were taken of pixels in each device's 11 arrays at five frequencies (1, 3, 10, and 100 kHz, and 1 MHz), and no frequency dependence was seen. Figure 2 shows data taken at 1 MHz at voltages for which the $C_{\rm inter-pixel}$-V curves are flat. We find that the capacitance of arrays with atoll p-stop design is relatively insensitive to the specific values of the implant dimensions for the design variations studied here. The capacitance of the common p-stop design shows the greatest variation with implant shape. As is shown in the figure, the capacitance of the five common p-stop designs decreases monotonically with array number. From this we conclude that the contributions of the gap width and the p-stop width to the inter-pixel capacitance appear

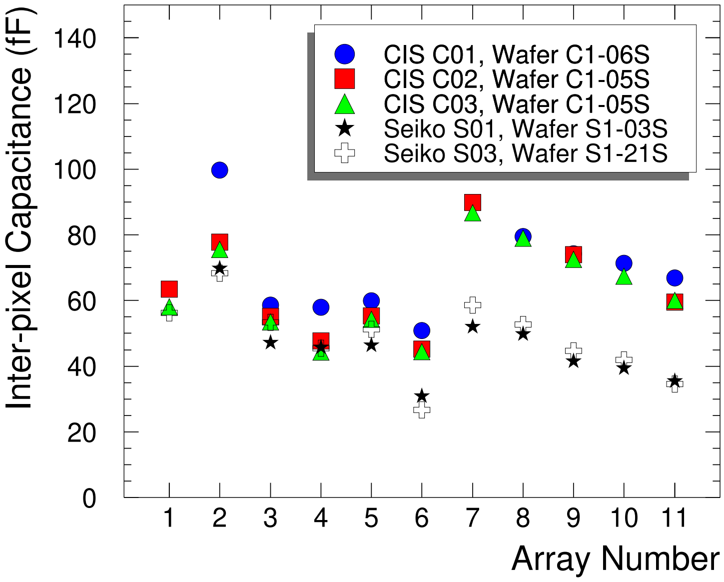

Fig. 2. Inter-pixel capacitance of the 11 arrays on n-on-n devices. The CiS devices were measured at bias voltages over the range 0–400 V and the Seiko, over the range 0–200 V.

to be comparable. The combined p-stop design has the smallest n^+ implant width (and consequently the largest distance between n^+ implants) and was observed to have the smallest capacitance of the designs tested. A linear relationship between the inter-pixel capacitance and the implant width describes the n-on-n data well, although some minor inconsistencies are observed. Of note is that Array 10 has slightly wider n^+ implants than Array 9 yet consistently shows a lower capacitance. Array 10 has wider gaps, so this result suggests that the size of the unimplanted gap plays a roll in the capacitance. This effect is described if one fits the data to Equation (1). Several of the n-on-n devices were irradiated beyond inversion by a fluence equivalent to 8×10^{14} cm^{-2} 1 MeV neutrons. Figure 3 shows the capacitance before and shortly after irradiation of all the arrays in a Seiko and a CiS sensor. While the values after irradiation are systematically higher than before, the size of the difference is consistent with the resolution on the measurement.

5 Temperature Dependence of Capacitance

The silicon pixel detectors in ATLAS will operate below room temperature, and it is likely that other future pixel systems will do so too. To quantify the temperature dependence of the inter-pixel capacitance, measurements were made at 1 MHz frequency for various temperatures from room temperature to below freezing. Open

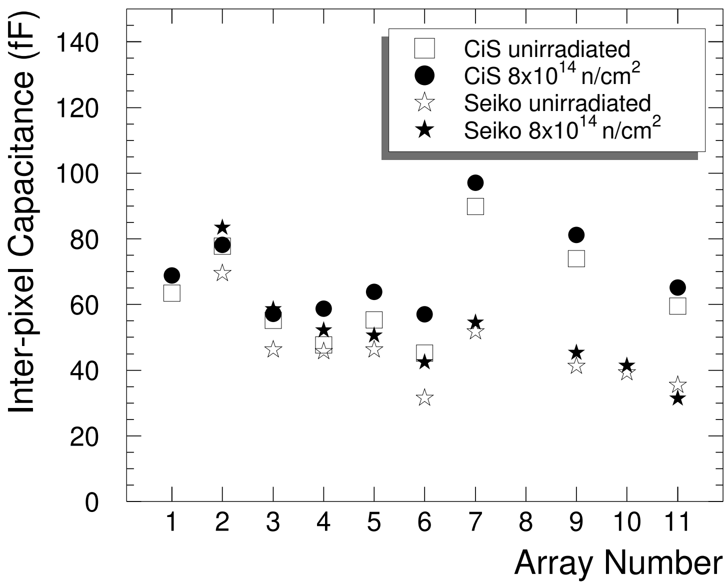

Fig. 3. Inter-pixel capacitance of the 11 arrays in one Seiko and one CiS Structure 6 device before and shortly after irradiation. The combined statistical and systematic error on each point is 5 fF.

corrections are not reliable for measurements taken in the thermal chamber. Unavoidable differences between the chamber environment and the probe station environment mean that systematic shifts between the two environments may occur. While relative changes in capacitance as a function of temperature are significant to this measurement in either environment, relative changes between the environments are not the object of this particular measurement. The results, displayed in Figure 4, show that in the range $+20°C$ to $-10°C$, capacitance measured at this frequency is temperature-independent. The temperature range and frequency value used in this measurement complement and extend those reported in two other studies (4; 6).

6 Conclusion

The inter-pixel capacitance of silicon pixel sensors with various implant widths, gaps, and p-stop designs was investigated. The inter-pixel capacitance was found to vary linearly with implant width for width-to-pitch ratios below 0.64. Some improvement in the description of the ratio is gained by including a term proportional to the inverse of the size of the gap between implants. A single parameterization is shown to adequately describe devices with three different p-stop designs. The observed dependence of the capacitance upon pixel width and gap size provides a means for predicting the inter-pixel capacitance of design variations not considered here. Designs suitable for

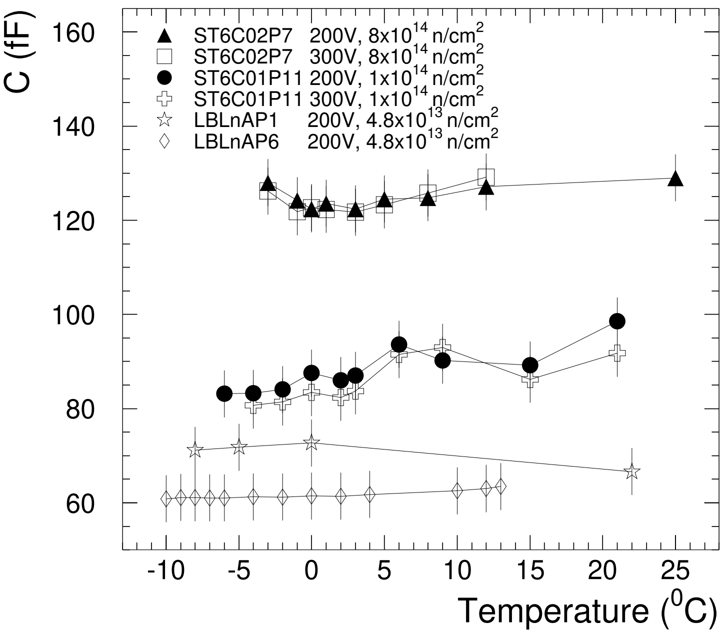

Fig. 4. Inter-pixel capacitance of n-on-n devices (whose labels begin with “ST6”) and p-on-n test structures (whose labels begin with “LBLn”), measured as a function of temperature. The legend in the figure indicates the bias voltage applied to, and the fluence received by, each sensor.

use in detectors at the LHC and the Tevatron have inter-pixel capacitance on the order of 60 fF to all neighbors and backplane capacitance of approximately 20 fF. Sensors irradiated to fluences relevant to LHC and Tevatron experiments displayed only a small systematic increase in the value of their inter-pixel capacitance. After irradiation, the measured inter-pixel capacitance saturates at lower voltages than prior to irradiation. No capacitance change is observed up to bias voltages of about 400 V; consequently these results are applicable to devices operating at high voltages as is anticipated at, for example, the LHC and Tevatron. No temperature dependence of the capacitance was observed for the range between room temperature and -10°C.

References

[1] Batignani, G., et al., *Nucl. Instr. and Meth.* A 277 (1989) 147.
[2] Barberis, E., et al., IEEE Trans. Nucl. Sci. 41 (1994) 785.
[3] Dabrowski, W., and K. Korbel, *Nucl. Instr. and Meth.* A 276 (1989) 270.
[4] Dezillie, B., Ph. D. thesis, University Joseph Fourier, 1997 (unpublished).
[5] Bacchetta, N., et al., *Nucl. Instr. and Meth.* A 409 (1998) 142.
[6] Borchi, E., et al., *Solid-State Electron.* 42, no. 11 (1998) 2093.