PIXEL SENSORS FOR ATLAS

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Abstract

The design and fabrication of the First Prototype Pixel Sensors for ATLAS has been completed. The wafers include two large rectangular structures, called tiles, as well as numerous smaller structures. Each tile accepts 16 readout chips and is compatible with the prototype module design. Most of the smaller structures are compatible with single readout chips. The designs of all of these prototype devices are explained with attention to the goals and constraints that guided design choices.

1 OVERVIEW OF THE ATLAS PIXEL SENSOR PROGRAM

The ATLAS Experiment at the CERN LHC will include a silicon pixel detector as its innermost tracking chamber. The detector will consist of three layers of rectangular sensors arranged in a cylindrical ("barrel") pattern coaxial with the beamline, and 2×5 layers of identical sensors assembled into disks. The detector will require 1508 barrel sensors and 720 disk sensors.

The pixel detector must survive for 10 years in the hostile radiation environment of the collider. The sensors closest to the beam will receive more than 10^{15} minimum ionizing particles/cm^2. The anticipated need to operate the sensors partially depleted after some point in their radiation lifetime is the dominant factor in the choice of n-type implants in n-type substrate. As radiation damage to the bulk will require increasingly higher operating voltages during the detector's lifetime, the requirement of operating these sensors at high voltage without electrical breakdown or microdischarge is important to the design. Some features of the design also reflect the desire to provide bias to every pixel without attaching the readout integrated circuit. This is expected to facilitate testing of the sensors prior to bonding and to guarantee a uniform electric field in the sensor active area in cases of failure of a bump bond. To minimize multiple scattering of tracks in this, the innermost of ATLAS's detection systems, the inner layer will be fabricated from sensors of 200μm thickness while the outer two layers and the disks will use 250μm sensors.

The production sensors for the ATLAS barrels will be 2 readout chips wide and 8 readout chips long. The readout chips will have 24 columns and 160 rows; each pixel cell will have dimensions $50 \times 300\mu\mathrm{m}^2$. Consequently, the active area for a barrel sensor will be 16.4×60.4 mm^2. The overall dimensions of the barrel sensor depend upon the module concept (still in development) but will lie in the range 16.4×62.4 mm^2 to 21.4×67.8 mm^2. Disk sensors will use the same technology as barrel sensors but will have a slightly different shape.[1]

The ATLAS pixel sensor design program includes fabrication of First Prototypes and Second Prototypes prior to production sensors. First Prototypes were designed in 1997, fabricated by CiS Institut für Mikrosensorik e.V. and Seiko Instruments Inc., and are now under study within ATLAS. The Second Prototypes are expected to be designed and ordered prior to January 1, 1999. Pre-production sensors will be designed and ordered in 1999 so that production sensors can be ready for assembly in 2000.

This document primarily concerns the First Prototypes. The First Prototype wafers contain 2 large structures, called Tile 1[1] and Tile 2[1, 2], 17 smaller sensors which examine additional design options and which can each be read out by a single amplifer chip, and a variety of process test structures. Design details of the two tiles and important features of some of the other structures are described below.

2 THE DESIGN OF THE FIRST PROTOTYPE SENSORS

2.1 Introduction

Figure 1 shows the layout of the (4-inch diameter, 280μm thick) First Prototype wafer. Figure 2 (including its Details A, B, C, D, E, and F) illustrates the n-side of Tile 1 after processing. Figure 3 shows a bond pad region. Figure 4 (including its Details A, B, and C) illustrates features of Tile 2. Figure 5 shows the Tile 2 i/o bus structure. Figure 6 shows the guard rings. Figure 7 illustrates the second metal pattern. Figure 8 shows the structure known as the bias grid.

2.2 Cell Geometry

On the accompanying figures, rows are labelled in the horizontal direction, columns in the vertical. The active area of each tile is divided into 16 units, a unit being defined as a group of pixels that use a common amplifier chip. The geometry of each pixel cell in the First Prototypes is characterized as follows:

- Number of pixel cells per readout chip: 164×18
- Total number of pixel cells: 47232 ($= 16 \times 164 \times 18$)
- Pixel cell dimensions: $50 \times 400 \mu\text{m}^2$. (This is larger than the production sensors' pitch in order to match the prototype electronics.)
- Cells that lie in columns which would not be adjacent to a chip's bump pads if they were 400μm long are elongated to 600μm. (See Figure 2, Detail B, and Figure 4, Detail B.)

2.3 n-side Isolation and Implant Dimensions

The principal difference between the two tiles is their technology for n-side isolation. Tile 2 uses p-spray[3], and Tile 1 uses p-stops. On the First Prototype wafers, regions that use the different isolation techniques are separated by a low precision mask.

In Tile 1, the n-type implants are isolated from one another by p-stops of the individual, or "atoll," design. This choice provides a low inter-pixel capacitance. Pairs of units are additionally surrounded by a common p-stop frame. The dimensions of Tile 1 implants are as follows:

- n^+ implant width: 23μm
- p^+ implant width: 5μm
- gap between n-type and p-type implants: 6μm
- gap between neighboring p^+ implants: 5μm.

Complete dimensions of the structures on Tile 2 are shown in Figure 4, Details A and B. For each pixel cell, the mask width of the central n-implant is 13μm, while the floating n-implant that surrounds it is 6μm wide. The spacing between those structures is 6μm. The floating implant serves to keep the distance between implants (and consequently the inter-implant electric field) small without compromising the relatively large distance, and hence low capacitance, between neighboring channels. In both tiles, corners are rounded to reduce electric fields. (See for example Figure 2, Detail D.)

2.4 n-side Guard Ring

The design of both tiles' n-side edge region (see Figure 6) is guided by the concern to minimize the possibility of electrical arcs between the sensor and the electronics which are only a bump's diameter away. There is an inner guard ring which consists in a metallized n^+ implant. On Tile 1 the implant has width 86.5μm; on Tile 2 the width is 90μm. On Tile 2 this inner ring can be used for biassing the whole array (see Section 2.12). Beyond the inner ring is an outer region covered with n^+ implant. The inner ring and outer region are separated by a gap. On Tile 1, that gap has total width 30μm and is unimplanted. To provide electrical isolation, a 10μm wide p-stop is placed in the center of the gap. On Tile 2, the gap is 8μm wide, and electrical isolation is provided by the p-spray implant which covers the whole device.

Contact pads to the n-type implant appear in the four corners of the tile. On each tile, one of these contact pads bears a label so that the orientation of the tile is uniquely specified. The outer n-implant is grounded externally.

2.5 p-side Guard Ring

Both tiles use the same design[4] for their p-side guard ring. The multi-guardring structure contains 22 rings with a pitch that varies from 20μm near the sensitive area to 50μm near the edge. The p-implant is 10μm wide in every ring while the gap increases from the center to the edge. The metal overlaps the implant by half of the gap width on the side of the ring facing the sensitive area. The entire guard ring structure is 525μm wide.

2.6 Double Metal

A second metal layer is being tested on 30% of the First Prototypes. Devices with and without double metal do not differ in any aspect of their design other than the double metal itself, the insulator, and the addition of vias to allow access through the insulator to first metal pads. In the First Prototype program, double-metal is being tested in some (redundant) busses on Tile 2 and as routing of signals from pixels at the edge of units to preamplifiers above neighboring implants. The busses run parallel to the long side of the sensor and are located between bump bond pads and the active area. Figure 5 shows a detail of the bus structure on Tile 2.

The narrowest line in Metal 2 is 10μm wide and 1.5–2.0 μm thick. The minimum Metal 2 spacing, which is not critical, is greater than 20μm. In the bus structure, Metal 2 has width 20–50 μm. The contact holes are $3 \times 10\mu\mathrm{m}^2$ in the masks. Metal on the first layer has thickness 1.2–1.5 μm. The insulator material varies with manufacturer: one vendor uses SiO_2; the other, polyimide. To maintain flatness of the bump pads, vias are not located beneath them. Figure 7 shows the second metal design.

Devices that have Metal 1 but not Metal 2 are completely functional. In the devices with both metal layers, the outermost four rows of pixels are not connected by bumps directly to their preamplifiers (i.e., their bump pads have no vias). Signals from pixels in those rows are instead routed in Metal 2 to neighboring pixels by using the same metal pattern as appears in Metal 1 in the sensor's central region.

2.7 As-cut Dimensions

The wafers containing the tiles are provided by their manufacturer without dicing in order that they may be bumped first. To accommodate the busses, Tile 2 is wider than Tile 1. After dicing, the dimensions of the tiles are:

Tile 1 (default): 18.6×62.6 mm^2, and

Tile 2 (default): 24.4×62.6 mm^2.

It may be necessary to increase the distance between the guard ring and scribeline in order to guarantee sufficient radiation hardness. To provide for this possibility, a second scribeline is included which would give the tiles the following dimensions:

Tile 1 (enlarged): 19.4×63.4 mm^2, and

Tile 2 (enlarged): 24.4×63.4 mm^2.

2.8 Metallization

On Tile 1, the first metal has width 14μm on the pixels. The metal width on the inner guard ring is 6μm narrower than the implant. The masks for the metallization over the implant of Tile 2 show a width of 12μm, 1μm less than the mask width of the implant.

2.9 Pads

The bond pads are twenty-sided polygons (approximating circles). On Tile 1 the implant has mask diameter 21μm, or processed diameter approximately 23μm. On Tile 2 the implant has mask diameter 18μm. On both tiles the first and second metals have diameter 20μm.

Bond pads are placed at the end of each pixel cell. This layout anticipates a mirrored electronics layout. The closely spaced bond pads are 50μm apart. (See Figure 2, Details A and B). A cross section of a bond pad region is included in Figure 3.

Some pixels have no bond pads. Those cells will have no preamplifier directly above them and so must have their signals routed to bond pads on pixels a few rows away in the same column. For both tiles, the routing will use a single metal layer. Figure 2 Details C and E show the routing for Tile 1 while Figure 4 Details B and C show it for Tile 2.

Bias pads are placed in several locations on the inner n^+ guard ring. They form two extra rows with the same 50μm pitch as the pixels have. See Figure 2, Detail F for an example of n-side bias pad placement. Probing pads are placed on the inner guard ring in the region between adjacent units (see Figure 2, Detail F).

2.10 p-side (Back Side) Design

This information concerns both tiles. A p^+ implant is continuous in the area covered by pixels. The aluminization has $30 \times 100 \mu\text{m}^2$ apertures to facilitate stimulating the cells from the p-side with a laser.

2.11 Passivation

The passivation must be compatible with technologies for applying bumps for bonding. A 1μm thick silicon nitride layer is used. The openings in the passivation for bump bonding have 12μm diameter.

2.12 Bias Grid

To maximize the yield on assembled modules, it is beneficial to test sensors under bias prior to attaching the amplifier chips. A bias grid is integrated into Tile 2 (see Figure 8) to allow every channel to be biased on a test stand without a chip and without contacting the implants directly. A bus between every pair of columns connects to a small n^+ implant “dot” near each pixel. When bias is applied (through a probe needle) to the grid via the inner guard ring of the n-side, every pixel is biased by punchthrough from its dot. (The use of p-spray facilitates this technology since the elimination of need for photolithographic registration permits the distance between n-implants to be small and hence keeps the punchthrough voltage low.) Once a chip has been attached, the grid is no longer used for biassing the cells. It nonetheless maintains any unconnected pixels (i.e., bad bumps) near ground potential. The punchthrough dot sacrifices 0.8% of the pixel’s active area.

2.13 Tolerances

The following tolerances are required:

- Uniformity of thickness: $\pm 10\mu$m
- Mask alignment: $\pm 2\mu$m

2.14 Sensor Electrical Properties

The following is a summary of the required electrical properties:

- Initial depletion voltage: 50–150V
- Initial maximum operating voltage: ≥ 200V
- Initial leakage current at $V_{\text{depletion}} + 10$V: < 100 nA/cm^2
- Initial oxide breakdown voltage: ≥ 100V.

2.15 Processing

The following processing requirements are made:

1. n^+ implant dose: $> 10^{14}/\text{cm}^2$.
2. concerning n-side isolation:
   - for Tile 1, the p^+ implant dose is $\geq 10^{13}/\text{cm}^2$.
   - for Tile 2, the p-spray effective dose in silicon is $(3.0 \pm 0.5) \times 10^{12}/\text{cm}^2$.
3. Back (p-side) contact dose: $> 10^{14}/\text{cm}^2$.
4. Implant depth after processing is $\geq 1\mu\text{m}$.

2.16 Radiation Hardness

The following specifications will be required of Second Prototype and production sensors. They are not required of First Prototype sensors. The properties of irradiated First Prototype sensors are nonetheless being studied.

The production sensors must have the following performance after an irradiation of 10^{15} p/cm^2:

1. Breakdown voltage: > 500 V.
2. Depletion voltage (for $300\mu\text{m}$ sensors): < 800 V.
3. Leakage current (measured at $-5°$ C) after one month of annealing at $20°$ C (for $300\mu\text{m}$ sensors): $< 125\mu\text{A}/\text{cm}^2$ or < 25 nA per pixel cell.

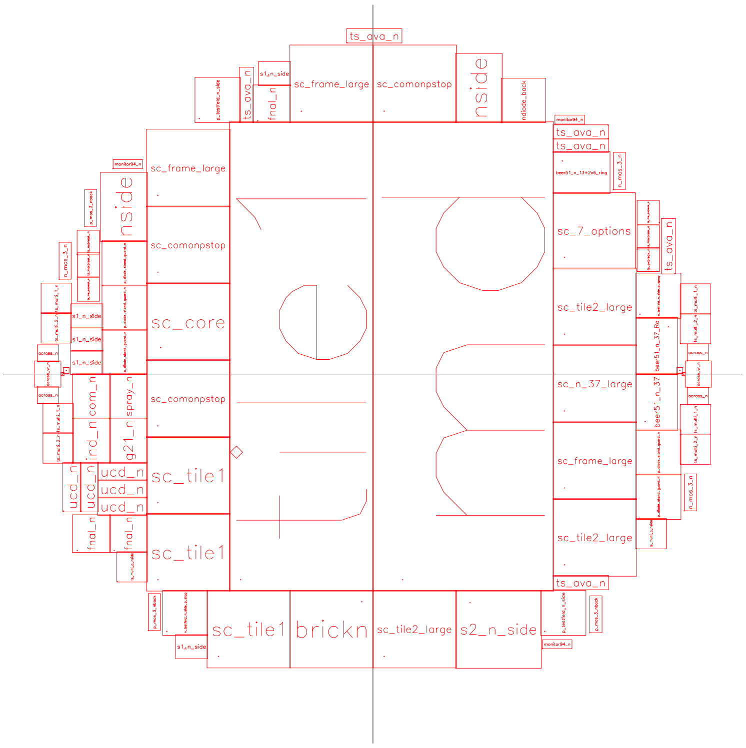
3 DESIGN VARIATIONS STUDIED ON SINGLE-CHIP SENSORS

On each wafer, three of the seventeen single-chip sensors have all of the design features of Tile 1. Three others have the features of Tile 2. Among the remainder, two evaluate a common p-stop design, one combines the common p-stop with p-spray, one studies a variety of p-stop geometries, and one evaluates three different bricking patterns. In the region of the wafer that uses p-spray, there are an additional 3 devices which explore techniques for minimizing cross talk, implementing bricking, and modifying implant geometries and gap sizes.

"Bricking" is the offsetting of pixel cells in neighboring rows by half a pixel length. Bricking improves the z resolution for double hits and reduces the cross talk coupling by distributing the capacitance over four neighboring cells rather than two. The challenge to the implementation of bricking comes from the fact that bricked sensor cells are not directly adjacent to the bump pads of the mirrored bump pad geometry of the (nonbricked) readout chip. Several solutions to this problem are being examined on the single-chip sensors. In one option, the bump pad is placed above a neighboring channel's implant and then routed in single metal to the implant which requires connection. This option produces cross talk between the two implants involved. In a second option, the routing between implants is accomplished in second metal. In the third option, called "partial bricking," routing is avoided entirely by staggering the implants only at their ends which have no bump pads. This option complicates pattern recognition slightly. The three bricking options are illustrated in Figures 9, 10, and 11.

4 TESTING

Acceptance testing is being done by ATLAS only. The wafer has test structures for monitoring flat band voltage, layer thickness, implant resistivity, aluminum sheet resistance, etching uniformity, and alignment.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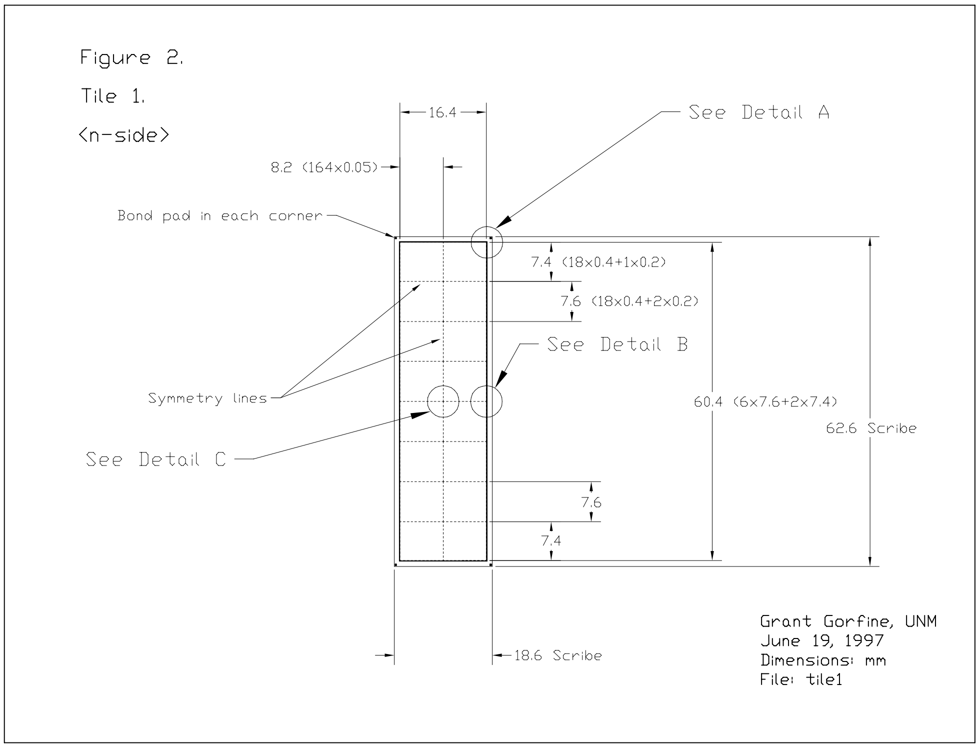


Figure 2: The Tile 1 concept.

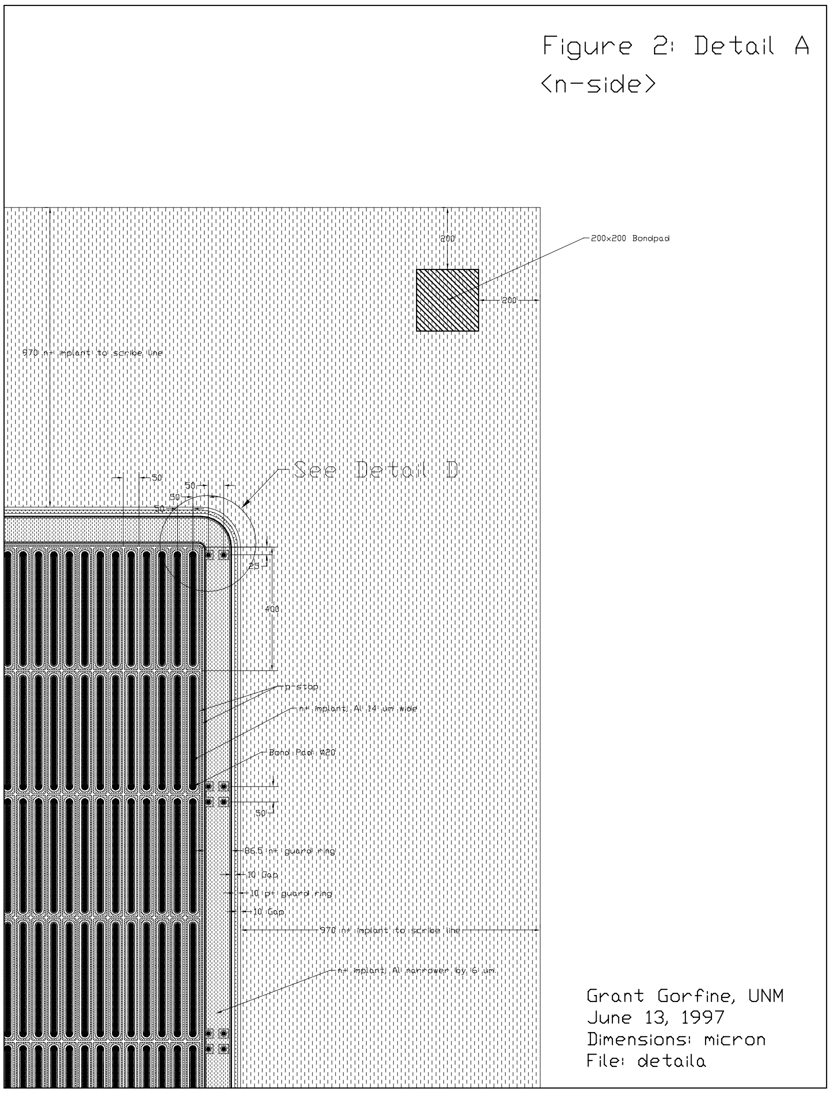


Figure 2a: Corner detail of Tile 1.

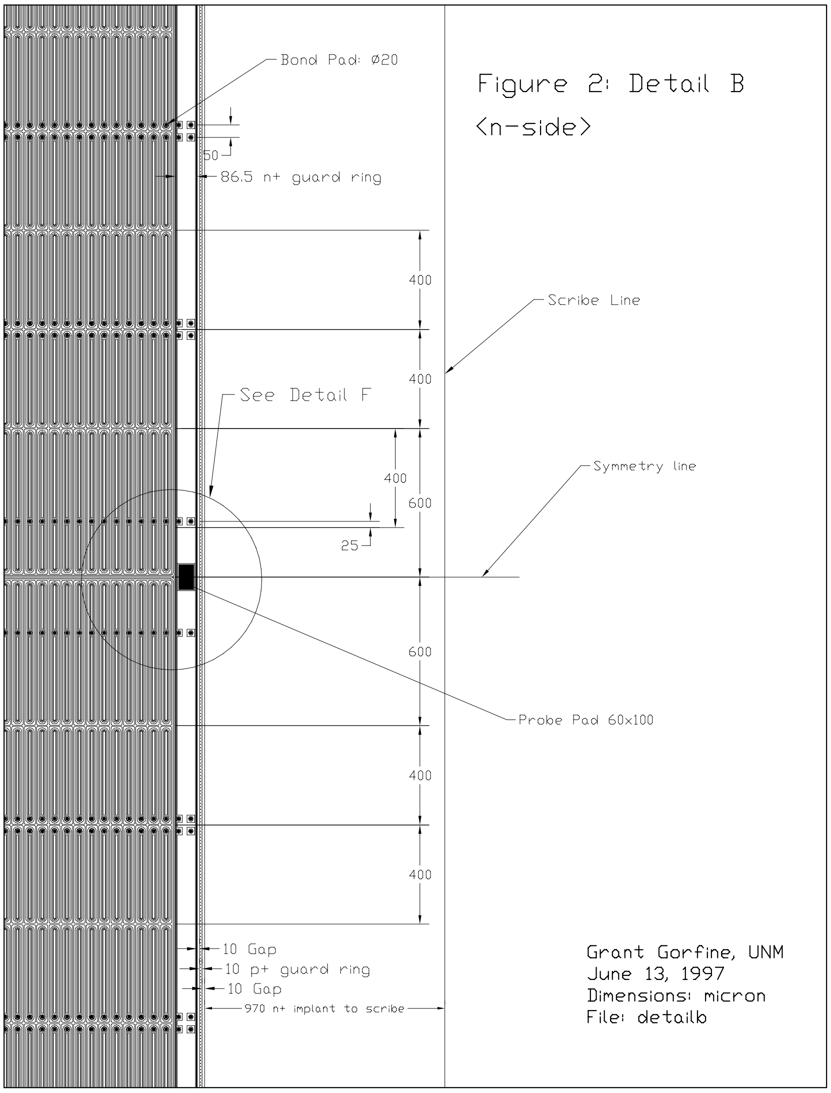


Figure 2b: Detail of Tile 1 showing a region between units in which cells of length 600 μm are used.

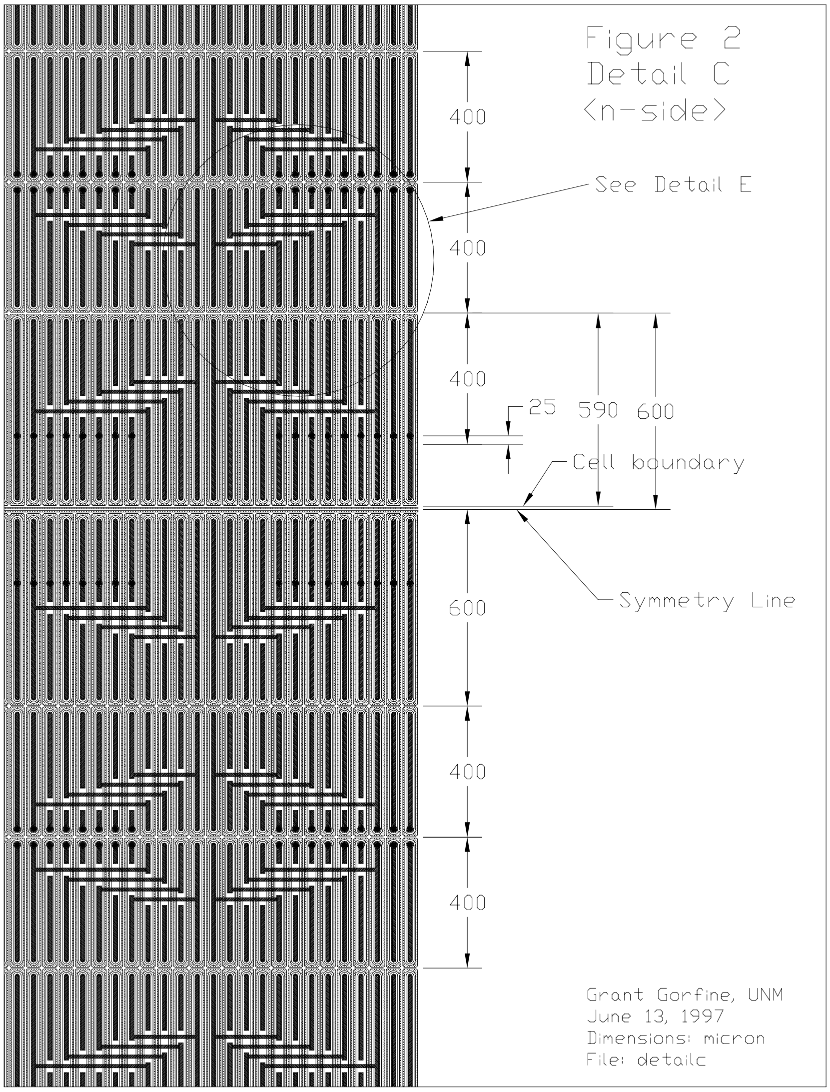


Figure 2c: Detail of Tile 1 showing first metal traces which route signals from implants at the edges of their units to the preamplifers above neighboring implants.

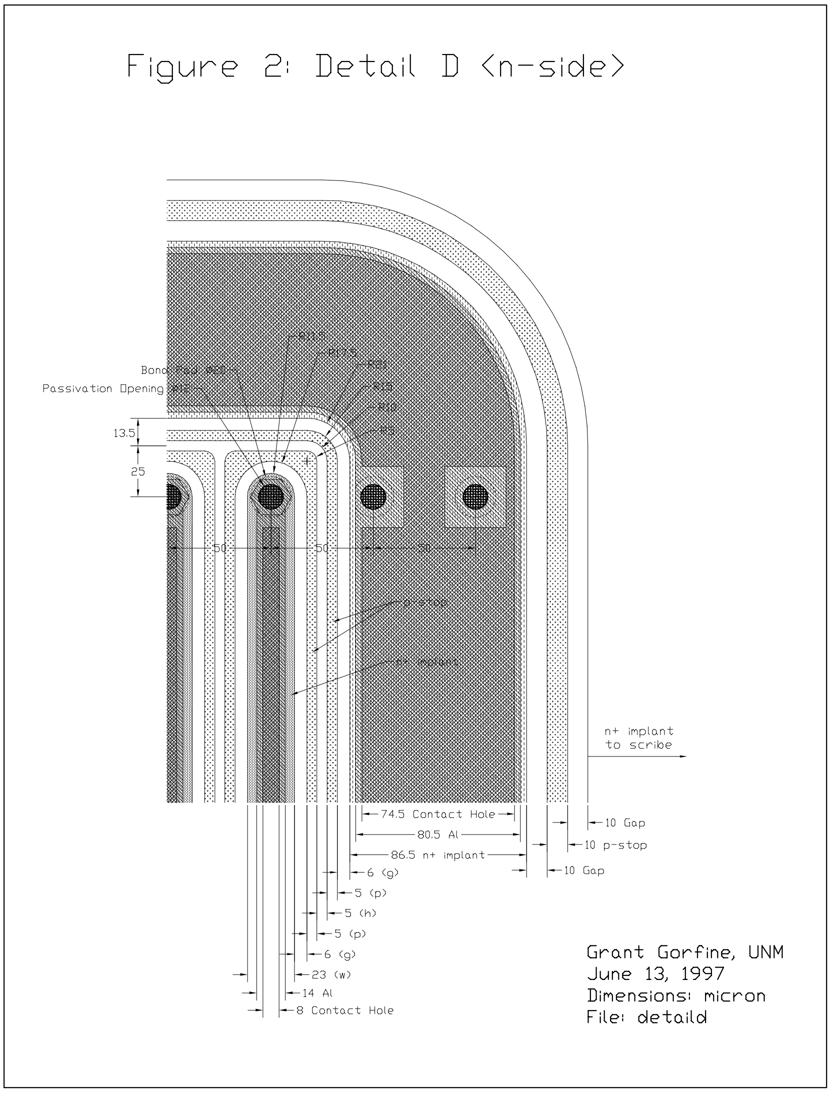


Figure 2d: Detail of Tile 1 showing the corner of the *n*-side guard ring and the isolation implants.

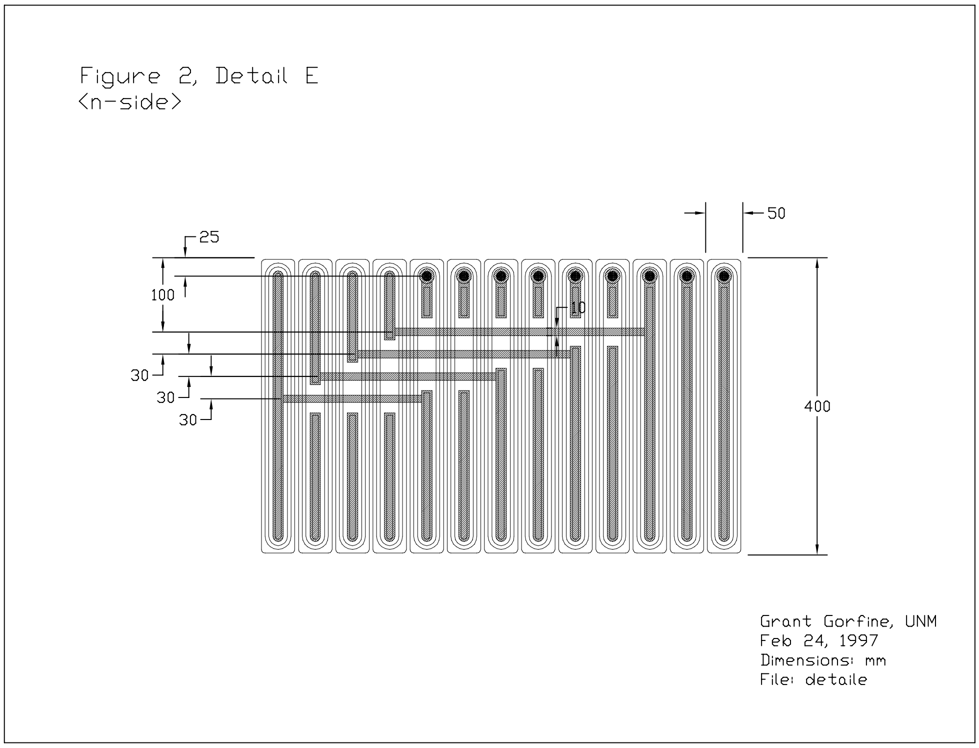


Figure 2e: Detail of Tile 1 showing the first metal near the edge of a unit.

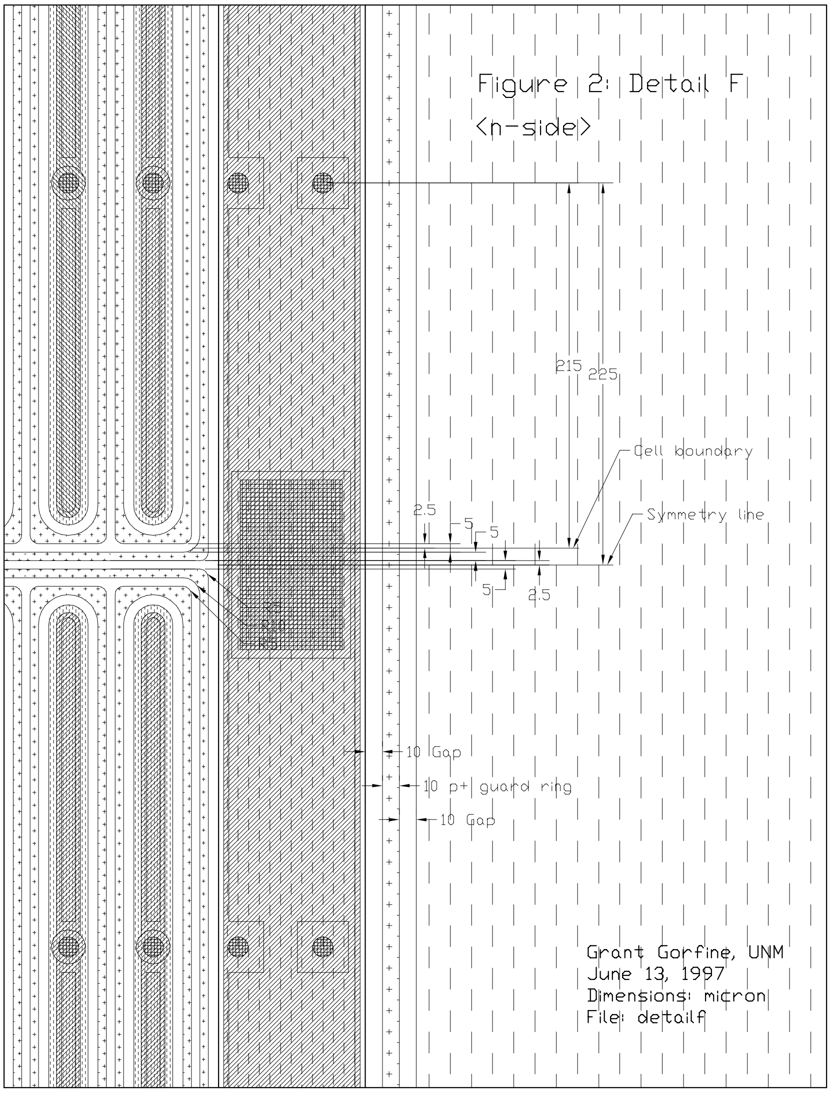
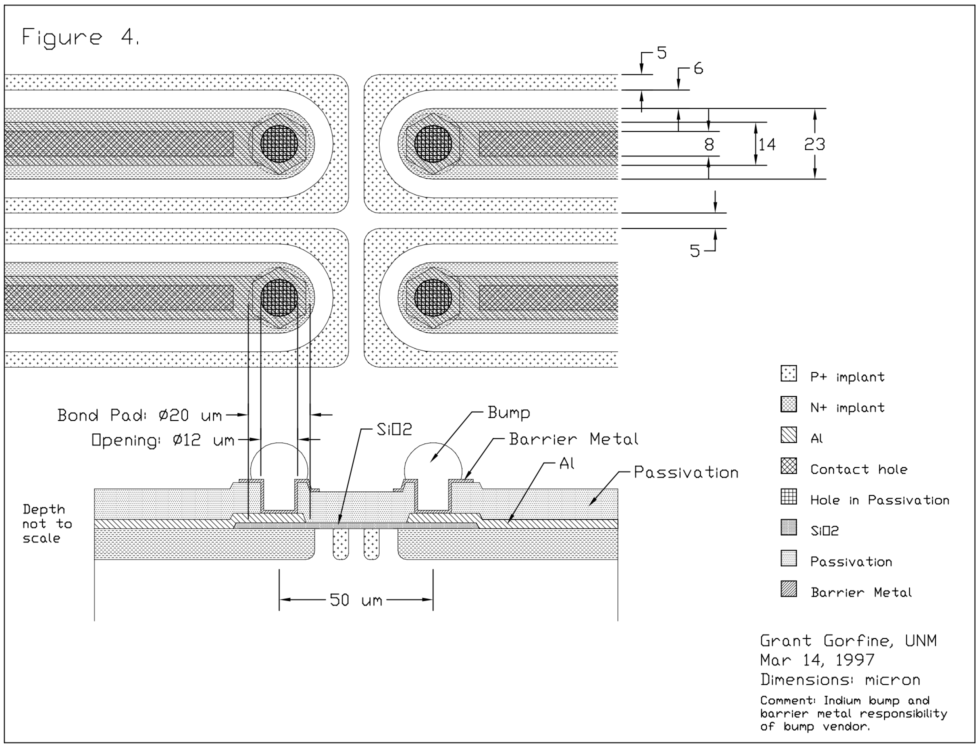


Figure 2f: Detail of Tile 1 showing the structure of isolation implants at the boundary between units.



Grant Gorfine, UNM
Mar 14, 1997
Dimensions: micron
Comment: Indium bump and barrier metal responsibility of bump vendor.

Figure 3: Concept of a Tile 1 bond pad region.

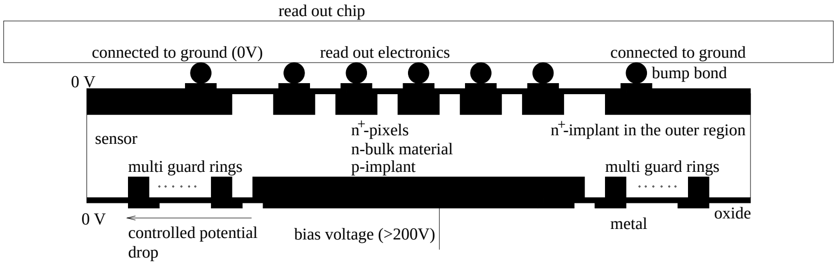


Figure 6: A cross section of a tile showing the guard rings.

Metal 2 Routing

Bias Ring Bump Pad without Via Bump Pad with Via

Metal 1 Metal 2 Via Passivation openings

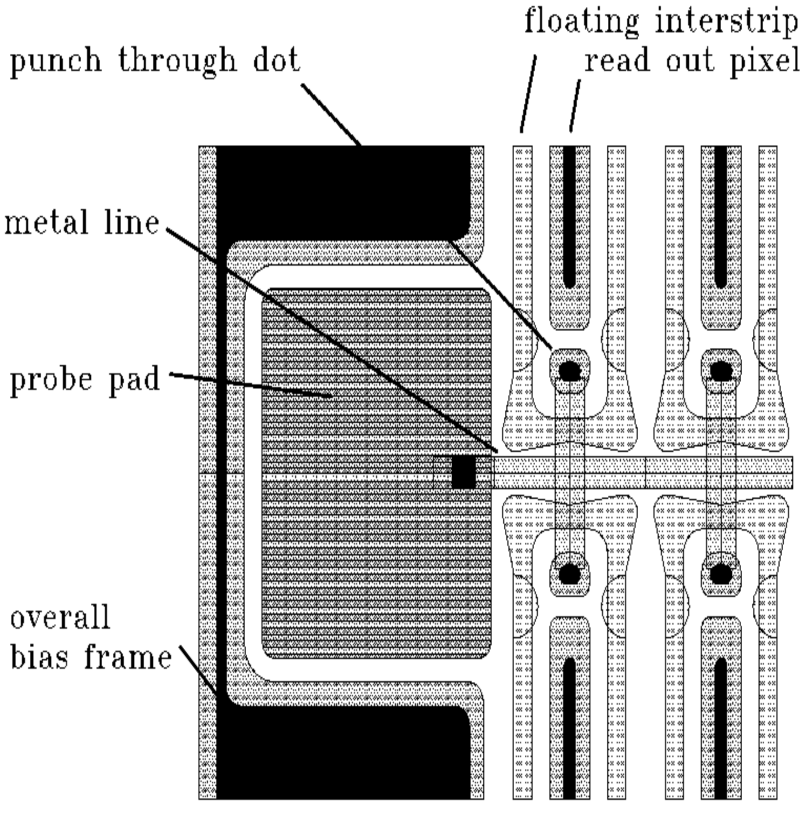


Figure 5, detail A

Figure 8: A section of the bias grid.

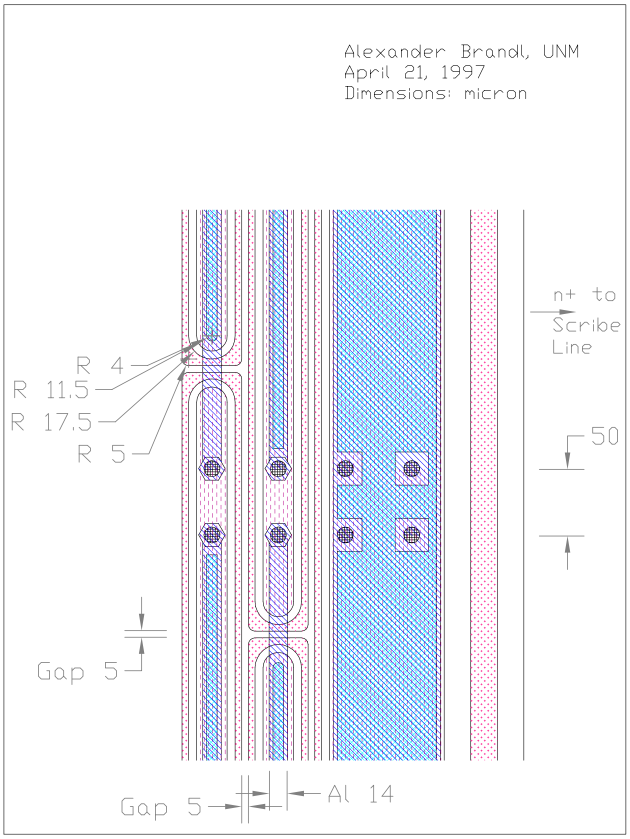


Figure 9: Bricking with single-metal routing.

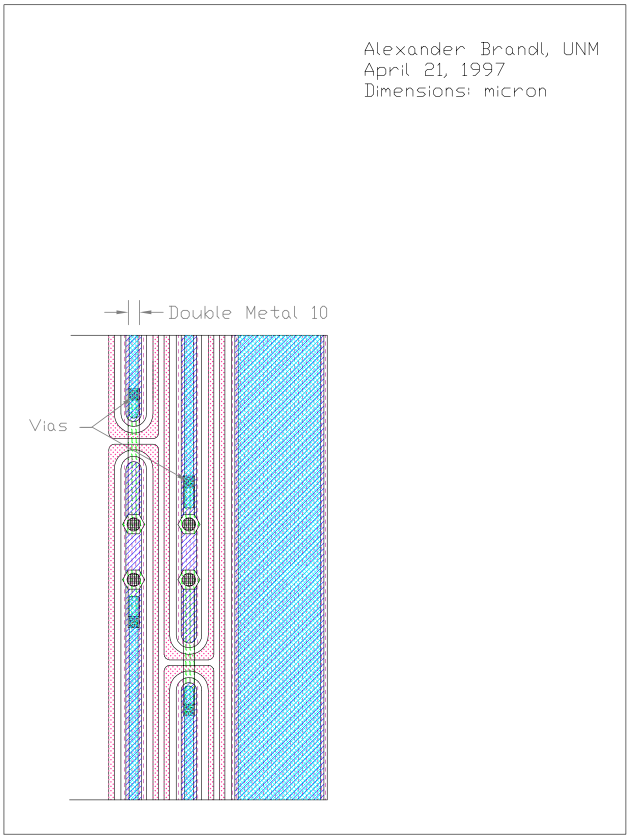


Figure 10: Bricking with double-metal routing.

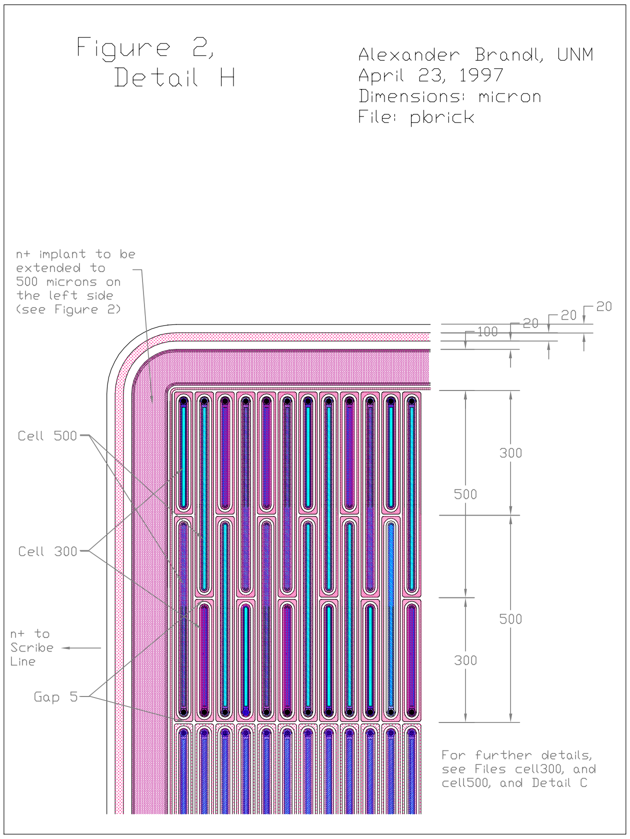


Figure 11: Partial bricking.

References

[1] The ATLAS Collaboration, *ATLAS Inner Detector Technical Design Report*, CERN/LHCC/97-17, April 1997.

[2] T. Rohe et al., *Sensor Design for the ATLAS-Pixel Detector*, Proc. Seventh Pisa Meeting on Advanced Detectors, Isola d'Elba, May 1997, to be published in *Nucl. Instr. and Meth.*

[3] R.H. Richter et al., *Nucl. Instr. and Meth.* A 377 (1996) 412-421.

[4] A. Bischoff et al., *Nucl. Instr. and Meth.* A 326 (1993) 27-37; B.S. Avset, *Nucl. Instr. and Meth.* A 377 (1996) 397-403.